EXHIBIT B

UNITED STATES DISTRICT COURT DISTRICT OF GUAM

NANYA TECHNOLOGY CORP. and NANYA TECHNOLOGY CORP. U.S.A.,

Case No. CV-06-00025

Plaintiffs.

DECLARATION OF KIMBERLY WILSON

v

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FUJITSU LIMITED and FUJITSU MICROELECTRONICS AMERICA, INC.,

Defendants.

I, Kimberly Wilson, hereby declare as follows:

- 1. My name is Kimberly Wilson and I am a travel agent with Canyon Creek Travel. I am over the age of 21 and am competent to make this declaration. All of the statements set forth herein are true and correct and are based on my professional practice and personal knowledge. The flight times and availability of flights are subject to change based upon daily and periodic fluctuations.
- 2. The flight time between Tokyo, Japan to Tamuning, Guam is approximately three to four hours. The geographic distance between Tokyo, Japan and Tamuning, Guam is approximately 1561 miles. The time difference between Tokyo, Japan and Tamuning, Guam is one hour.
- 3. Based upon figures published by the Guam Visitors Bureau, in 2006, of the approximately 1.2 million visitors to Guam, approximately 79% came from Japan. The second largest number of visitors to Guam came from Korea with approximately 9%. There are nine cities in Japan with direct flights to Guam. In contrast, there are only three cities in Japan with direct flights to San Francisco, California.

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- 3. The flight time between Tokyo, Japan to San Francisco, California is approximately nine to ten hours. The geographic distance between Tokyo, Japan and San Francisco, California is approximately 5131 miles. The time difference between Tokyo, Japan and San Francisco, California is sixteen hours. Thus, the distance between Tokyo, Japan and San Francisco, California is over three times as far as between Tokyo, Japan and Tamuning, Guam and it takes approximately three times as long to get from Tokyo to San Francisco as it takes to get from Tokyo to Guam.
- The flight time between Taipei, Taiwan and Tamuning, Guam is approximately three to four hours. The geographic distance between Taipei, Taiwan and Tamuning, Guam is approximately 1721 miles. The time difference between Taipei, Taiwan and Tamuning, Guam is two hours.
- 5. The flight time between Taipei, Taiwan and San Francisco, California is approximately eleven to twelve hours. The geographic distance between Taipei, Taiwan and San Francisco, California is approximately 6450 miles. The time difference between Taipei, Taiwan and San Francisco, California is fifteen hours. Thus, the distance between Taipei, Taiwan and San Francisco, California is almost four times as far as between Taipei, Taiwan and Tamuning, Guam and it takes approximately three times as long to get from Taipei to San Francisco as it takes to get from Taipei to Guam.
- 6. Additionally, the geographic distance between San Francisco International Airport and the federal courthouse in Oakland is approximately 22 miles and takes approximately 40 minutes to travel. The geographic distance between the Guam airport and the federal courthouse for the District of Guam is approximately less than five miles and takes approximately 10 minutes to travel. Thus, overall, the total travel time from Tokyo to the federal

courthouse in Oakland is over three times longer than it is from Tokyo to the federal courthouse in Guam. Also, the overall, the total travel time from Taipei to the federal courthouse in Oakland is approximately four times longer than it is from Taipei to the federal courthouse in Guam. I DECLARE UNDER PENALTY OF PERJURY UNDER THE LAWS OF THE UNITED STATES OF AMERICA THAT THE FOREGOING IS TRUE AND CORRECT. **DAY OF MAY, 2007** SIGNED ON THE **SIGNATURE** PRINTED NAME TITLE

EXHIBIT C

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UNITED STATES DISTRICT COURT DISTRICT OF GUAM

NANYA TECHNOLOGY CORP. and NANYA TECHNOLOGY CORP. U.S.A., Plaintiffs.

Case No. CV-06-00025

DECLARATION IN SUPPORT OF PLAINTIFFS' RESPONSE TO DEFENDANTS' MOTION TO IMMEDIATELY TRANSFER FOR CONVENIENCE

FUJITSU LIMITED and FUJITSU MICROELECTRONICS AMERICA, INC., Defendants.

- 1. Nanya Technology Corporation ("NTC") is a Taiwanese corporation having its principal place of business in Hwa Ya Technology Park, 669, Fu Hsing 3rd Rd., Kucishan, Taoyuan, Taiwan, Republic of China.
- 2. Nanya Technology Corporation U.S.A. ("NTC USA") is a wholly owned subsidiary of NTC. NTC USA is NTC's sales office for America. NTC USA's employees do not conduct any relevant research and/or production of the patents-in-suit or accused devices.
- Several of NTC U.S. Patents are at issue in this matter, including U.S Patent No. 3. 6,225,187 ("the '187 Patent"); U.S. Patent No. 6,426,271 ("the '271 Patent"); and U.S. Patent No. 6,790,765 ("the '765 Patent").
- 4 Tse-Yao Huang, Yun-Sen Lai, Yi-Nan Chen, Hsien-Wen Liu, and Hul-Min Mao, inventors of the '187, '271, and '765 Patents all reside in Taiwan. All documents related to the original design and manufacturing of the invention described in the '187, '271, and '765 Patents. including inventor's notes, product specifications, conception, and reduction to practice (to the extent such documents exist), are located in Talwan.
- 5. Defendants have accused NTC and NTC's semiconductor memory products of infringing certain Fujitsu Ltd. U.S. Patents. The majority of documents related to the original design and manufacturing of NTC's semiconductor memory products, including engineer's notes

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and production specifications, are located in Talwan. The majority of documents related to NTC's sales, offers to sell, use, importation, exportation, and distribution of its semiconductor memory products are located in Taiwan. The majority of engineers and persons with knowledge of NTC's semiconductor memory products reside in Taiwan.

- Representatives from NTC and Fujitsu Ltd. participated in license negotiations from 1999 to 2005 with respect to the Fujitsu Ltd. U.S. patents-in-suit, all of which occurred in either Taiwan or Japan. All representatives from NTC who participated in these license negotiations reside in Taiwan.
- NTC is relatively small compared to Fujitsu Ltd. NTC's engineers and other NTC 7. personnel with knowledge of relevant facts have limited available time to travel for depositions, hearings, trial, and other proceedings. A venue closer to Taiwan would permit NTC personnel to more efficiently and easily participate in such proceedings. Air travel from Taiwan to Guam takes about three hours compared to eleven hours to California and does not require crossing the International Date Line. Conducting this lawsuit in Guam compared to California would permit NTC personnel to return to work after participating in such proceedings with substantially less delay and expanse.

I DECLARE UNDER PENALTY OF PERJURY UNDER THE LAWS OF THE UNITED STATES OF AMERICA THAT THE FOREGOING IS TRUE AND CORRECT. DAY OF MAY, 2007 SIGNED ON THE Zw

SIGNATURE

PRINTED NAME

TITLE

EXHIBIT D

UNITED STATES DISTRICT COURT DISTRICT OF GUAM

NANYA TECHNOLOGY CORP. and NANYA TECHNOLOGY CORP. U.S.A.,

Case No. CV-06-00025

Plaintiffs.

DECLARATION OF ASHLEY NICOLE MOORE

V.

FUJITSU LIMITED and FUJITSU MICROELECTRONICS AMERICA, INC.,

Defendants.

I, ASHLEY NICOLE MOORE, DECLARE UNDER PENALTY OF PERJURY THAT THE FOLLOWING IS TRUE AND CORRECT:

- 1. I am registered to practice before the United States Patent and Trademark Office. It is my understanding that the patents-in-suit include the following: U.S. Patent No. 4,384,918, U.S. Patent No. 4,458,336, U.S. Patent No. 4,527,070, U.S. Patent No. 4,539,068, U.S. Patent No. 4,641,166, U.S. Patent No. 4,692,689, U.S. Patent No. 4,801,989, U.S. Patent No. 5,227,996, U.S. Patent No. 5,339,273, U.S. Patent No. 5,397,432, U.S. Patent No. 5,688,712, U.S. Patent No. 5,841,731, U.S. Patent No. 6,104,486, U.S. Patent No. 6,292,428, and U.S. Patent No. 6,320,819.
- 2. U.S. Patent No. 4,384,918 identifies Naomichi Abe as the sole inventor and Fujitsu Limited as the assignee. Naomichi Abe is identified as residing in Tokyo, Japan, and Fujitsu Limited is identified as residing in Kawasaki, Japan. A true and correct copy of U.S. Patent No. 4,384,918's front page, which bears this information, is attached hereto as Exhibit A.
- 3. U.S. Patent No. 4,458,336 identifies Yoshihiro Takemae as the sole inventor and Fujitsu Limited as the assignee. Yoshihiro Takemae is identified as residing in Yokohama, Japan, and Fujitsu Limited is identified as residing in Kawasaki, Japan. A true and correct copy of U.S. Patent No.

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4,458,336's front page, which bears this information, is attached hereto as Exhibit B. Also attached as Exhibit C is a declaration signed by Yoshihiro Takemae confirming under penalty of perjury the inventor's residence in Japan.

- 4. U.S. Patent No. 4,527,070 identifies Shougo Matsui, Yoshimitu Mashima, and Kenichi Kobayashi as the inventors and Fujitsu Limited as the assignee. Shougo Matsui is identified as residing in Sagamihara, Japan, Yoshimitu Mashima is identified as residing in Kawasaki, Japan, Kenichi Kobayashi is identified as residing in Tokyo, Japan, and Fujitsu Limited is identified as residing in Kawasaki, Japan. A true and correct copy of U.S. Patent No. 4,527,070's front page, which bears this information, is attached hereto as Exhibit D. Also attached as Exhibit E is a declaration signed by Shougo Matsui, Yoshimitu Mashima, and Kenichi Kobayashi confirming under penalty of perjury each inventor's residence in Japan.
- 5. U.S. Patent No. 4,539,068 identifies Mikio Takagi, Kanetake Takasaki, and Kenji Koyama as the inventors and Fujitsu Limited as the assignee. Mikio Takagi is identified as residing in Kawasaki, Japan, Kanetake Takasaki is identified as residing in Tokyo, Japan, Kenji Koyama is identified as residing in Yokosuka, Japan, and Fujitsu Limited is identified as residing in Kawasaki, Japan. A true and correct copy of U.S. Patent No. 4,539,068's front page, which bears this information, is attached hereto as Exhibit F. Also attached as Exhibit G is a declaration signed by Mikio Takagi, Kanetake Takasaki, and Kenji Koyama confirming under penalty of perjury each inventor's residence in Japan.
- 6. U.S. Patent No. 4,641,166 identifies Yoshihiro Takemae, Tomio Nakano, and Kimiaki Sato as the inventors and Fujitsu Limited as the assignee. Yoshihiro Takemae is identified as residing in Tokyo, Japan, Tomio Nakano is identified as residing in Kawasaki, Japan, Kimiaki Sato is identified as residing in Tokyo, Japan, and Fujitsu Limited is identified as residing in Kawasaki, Japan. A true and correct copy of U.S. Patent No. 4,641,166's front page, which bears this information, is attached

hereto as Exhibit H. Also attached as Exhibit I is a declaration signed by Yoshihiro Takemae, Tomio Nakano, and Kimiaki Sato confirming under penalty of perjury each inventor's residence in Japan.

- 7. U.S. Patent No. 4,692,689 identifies Yoshihiro Takemae as the sole inventor and Fujitsu Limited as the assignee. Yoshihiro Takemae is identified as residing in Tokyo, Japan, and Fujitsu Limited is identified as residing in Kawasaki, Japan. A true and correct copy of U.S. Patent No. 4,692,689's front page, which bears this information, is attached hereto as Exhibit J.
- 8. U.S. Patent No. 4,801,989 identifies Masao Taguchi as the sole inventor and Fujitsu Limited as the assignee. Masao Taguchi is identified as residing in Sagamihara, Japan, and Fujitsu Limited is identified as residing in Kanagawa, Japan. A true and correct copy of U.S. Patent No. 4,801,989's front page, which bears this information, is attached hereto as Exhibit K. Also attached as Exhibit L is a declaration signed by Masao Taguchi confirming under penalty of perjury the inventor's residence in Japan.
- 9. U.S. Patent No. 5,227,996 identifies Toshiya Uchida as the sole inventor and Fujitsu Limited as the assignee. Toshiya Uchida is identified as residing in Kawasaki, Japan, and Fujitsu Limited is identified as residing in Kanagawa, Japan. A true and correct copy of U.S. Patent No. 5,227,996's front page, which bears this information, is attached hereto as Exhibit M. Also attached as Exhibit N is a declaration signed by Toshiya Uchida confirming under penalty of perjury the inventor's residence in Japan.
- 10. U.S. Patent No. 5,339,273 identifies Masao Taguchi as the sole inventor and Fujitsu Limited as the assignee. Masao Taguchi is identified as residing in Kawasaki, Japan, and Fujitsu Limited is identified as residing in Kanagawa, Japan. A true and correct copy of U.S. Patent No. 5,339,273's front page, which bears this information, is attached hereto as Exhibit O. Also attached as Exhibit P is a declaration signed by Masao Taguchi confirming under penalty of perjury the inventor's residence in Japan.

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- 11. U.S. Patent No. 5,397,432 identifies Jun-ichi Konno, Keisuke Shinagawa, Toshiyuki Ishida, Takahiro Ito, Tetsuo Kondo, Fukashi Harada, and Shuzo Fujimura as the inventors and Fujitsu Limited as the assignee. Jun-ichi Konno is identified as residing in Kuwana, Japan, Keisuke Shinagawa is identified as residing in Kawasaki, Japan, Toshiyuki Ishida is identified as residing in Kawasaki, Japan, Takahiro Ito is identified as residing in Kawasaki, Japan, Tetsuo Kondo is identified as residing in Kawasaki, Japan, Fukashi Harada is identified as residing in Kuwana, Japan, Shuzo Fujimura is identified as residing in Tokyo, Japan, and Fujitsu Limited is identified as residing in Kawasaki, Japan. A true and correct copy of U.S. Patent No. 5,397,432's front page, which bears this information, is attached hereto as Exhibit Q. Also attached as Exhibit R is a declaration signed by Junichi Konno confirming under penalty of perjury the inventor's residence in Japan.
- 12. U.S. Patent No. 5,688,712 identifies Taiji Ema and Toshimi Ikeda as the inventors and Fujitsu Limited as the assignee. Taiji Ema is identified as residing in Kawasaki, Japan, Toshimi Ikeda is identified as residing in Kawasaki, Japan, and Fujitsu Limited is identified as residing in Kanagawa, Japan. A true and correct copy of U.S. Patent No. 5,688,712's front page, which bears this information, is attached hereto as Exhibit S. Also attached as Exhibit T is a declaration signed by Taiji Ema confirming under penalty of perjury the inventor's residence in Japan.
- 13. U.S. Patent No. 5,841,731 identifies Naoharu Shinozaki as the sole inventor and Fujitsu Limited as the assignee. Naoharu Shinozaki is identified as residing in Kawasaki, Japan, and Fujitsu Limited is identified as residing in Kawasaki, Japan. A true and correct copy of U.S. Patent No. 5,841,731's front page, which bears this information, is attached hereto as Exhibit U. Also attached as Exhibit V is a declaration signed by Naoharu Shinozaki confirming under penalty of perjury the inventor's residence in Japan.
- 14. U.S. Patent No. 6,104,486 identifies Hiroshi Arimoto as the sole inventor and Fujitsu Limited as the assignee. Hiroshi Arimoto is identified as residing in Kawasaki, Japan, and Fujitsu

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Limited is identified as residing in Kawasaki, Japan. A true and correct copy of U.S. Patent No. 6,104,486's front page, which bears this information, is attached hereto as Exhibit W.

- 15. U.S. Patent No. 6,292,428 identifies Hiroyoshi Tomita and Tatsuya Kanda as the inventors and Fujitsu Limited as the assignee. Hiroyoshi Tomita is identified as residing in Kawasaki, Japan, Tatsuya Kanda is identified as residing in Kawasaki, Japan, and Fujitsu Limited is identified as residing in Kanagawa, Japan. A true and correct copy of U.S. Patent No. 6,292,428's front page, which bears this information, is attached hereto as Exhibit X. Also attached as Exhibit Y is a declaration signed by Hiroyoshi Tomita and Tatsuya Kanda confirming under penalty of perjury each inventor's residence in Japan.
- 16. U.S. Patent No. 6,320,819 identifies Hiroyoshi Tomita and Tatsuya Kanda as the inventors and Fujitsu Limited as the assignee. Hiroyoshi Tomita is identified as residing in Kawasaki, Japan, Tatsuya Kanda is identified as residing in Kawasaki, Japan, and Fujitsu Limited is identified as residing in Kawasaki, Japan. A true and correct copy of U.S. Patent No. 6,320,819's front page, which bears this information, is attached hereto as Exhibit Z. Also attached as Exhibit AA is a declaration signed by Hiroyoshi Tomita and Tatsuya Kanda confirming under penalty of perjury each inventor's residence in Japan.
- I personally obtained and confirmed all of the foregoing information from records 17. retrieved from the United States Patent and Trademark Office.
- 18. Upon and information and belief, Defendant Fujitsu Limited, is a Japanese corporation, having its principal place of business at Shiodome City Center, 1-5-2 Higashi-Shimbashi, Minato-ku, Tokyo 105-7123, Japan.
- 19. Upon and information and belief, Defendant Fujitsu Microelectronics America, Inc. is a wholly owned subsidiary of Fujitsu Ltd. and is headquartered and has its principal place of business at 1250 E. Arques Avenue, M/S 333, Sunnyvale, California 94088-3470.

United States Patent [19]

[11]

4,384,918

Abe

[45] May 24, 1983

[54]	METHOD AND APPAR ETCHING AND ELECT CHUCKING DEVICE U	ROSTATIC
[75]	Inventor: Nasmichi Ab	e, Tokyo, Japan
[73]	Assignee: Pajitsu Limit	ed, Kawasaki, Japan
[21]	Appl. No.: 304,902	•
[22]	Filed: Sep. 23, 1981	,
[30]	Foreign Application	Priority Data
Sep Oc	p. 30, 1980 [JP] Japan lct. 8, 1980 [JP] Japan	55-13625: 55-141040
[51] [52]	Int. CL ³	C23C 15/06 156/643; 156/345 92 B; 204/298; 361/234
[58]	Field of Search	72 B; 204/256; 361/254 156/345, 643 R, 1 M; 271/18.1, 18.2 1691; 361/234; 118/500
[56]	. References (Sted
	U.S. PATENT DO	CUMENTS

3,634,740	1/1972	Stepeko	361/23
3,916,270	10/1975	Wachtuer et al.	361/23
4,184,188	1/1980	Briglia	361/23
4,282,267	1/1981	Kuyel	M/192 I
4,292,153	9/1981	Kudo et al	204/29
4,313,783	2/1980	Davice et al.	156/34
4,324,611	4/1982	Vogel et al.	204/29

OTHER PUBLICATIONS

"Microetch Ion Beam Milling", VEECO Co. Catalog, pp. 1-29.

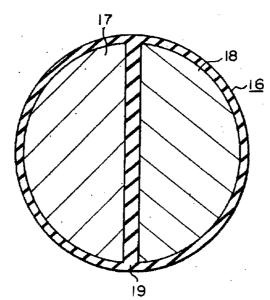
"Wafer Coaling . . . Btching", Conference Paper of Precision Machine Society, (1979), pp. 193-194.

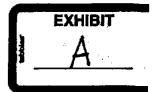
Primary Examiner-Jerome W. Massie Attorney, Agent, or Firm-State & Halsey

[57] ABSTRACT

An electrostatic chucking device is positioned on a supporting base, the temperature of which is maintained at a predetermined value, the device having an insulator, and a pair of plane electrodes on the insulator, and a material being chucked on the bottom surface of the top surface of the insulator, wherein the sum of the area of portions of the pair of plane electrodes facing the direction of the material being approximately equal to the contact area between the material and the insulator, and wherein a voltage is applied between the plane electrodes from an external power source, thereby effectively electrostatically chucking the material to the supporting base. A method and an apparatus for dry etching of a material having at least a conductive portion therein, the material being chucked by using said electrostatic chucking device mounted on a supporting base, the temperature of which is maintained at a predetermined value, in at least one of a sputter etching apparatus, a reactive sputter etching apparatus, or a plasma etching apparatus, whereby the material is indirectly chucked to the supporting base, the heat conductivity between the material and the supporting base is increased, the temperature of the material is controlled effectively, and the material can be held invertedly in the horizontal plane or vertically.

18 Claims, 10 Drawing Figures





United States Patent [19]

Takemae

[11] Patent Number:

4,458,336

[45] Date of Patent:

Jul. 3, 1984

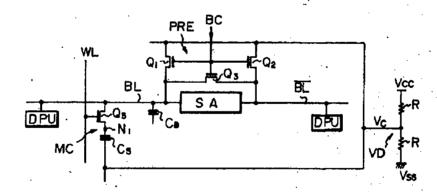
[54]	SEMICON	DUCTOR MEMORY CIRCUIT
[75]	Investor:	Yoshihiro Takemaa, Yokohama, Japan
[73]	Assigned:	Fujitsu Limited, Kawasaki, Japan
[21]	Appl. No.:	313,616
[22]	Filed:	Oct. 21, 1981
[30]	Foreig	n Application Priority Data
		P] Japan
[52]	U.S. Cl	
[56]		References Cited
	U.S. !	PATENT DOCUMENTS
	4,195,357 3/	1977 Harland

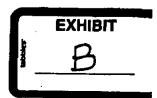
Primary Examiner-Joseph A. Popek Attorney, Agent, or Firm-Steas & Halsey

[57] ABSTRACT

A semiconductor memory circuit is disclosed, which includes: word lines, bit lines and memory cells at each cross point of the word lines and the bit lines. Each memory cell including a capacitor, having a first electrode and a second electrode, and a transfer-gate transistor connected in series with the capacitor at the first electrode thereof. The memory circuit also includes pre-charge circuits each charging one corresponding bit line to a predetermined pre-charge voltage level by using a memory power source and sense ampliflers each amplifying the voltage level developed at one corresponding bit line so as to have a high voltage level or a low voltage level in accordance with the charge stored in each corresponding capacitor. Additionally included are a first circuit which supplies the pre-charge voltage to the pre-charge circuit, the level of the pre-charge voltage is in the middle between the high voltage level and the low voltage level, and a second circuit which supplies a predetermined voltage to the capacitor at its second electrode. Preferably the predetermined voltage supplied from the second circuit is same as the voltage supplied from the first circuit.

12 Claims, 15 Drawing Figures





Petent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless a deplays a valid OMS control number.

Japanese Language Declaration (日本語宣言者)

会化状: 別は下記の発明者として、本出館に関する一切の 予視する米特許研究所に対して選行する中華出または代理人 として、下記の者を指名いたします。(弁護士、または代理 人の氏名及び登録番号を明記のこと) POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s), to presente this application and transact all business in the Patent and Trademark Office connected therewith (list name and registration number)

古城进行是

And I hereby appoint as principal asterneys: David T. Nilaido, Rag. No. 22,663; Charies M. Marmalssein, Reg. No. 25,895; George B. Oram, Jr., Reg. No. 27,951; Robert B. Murray, Reg. No. 22,960; B. Marcle Emas, Reg. No. 32,131; Douglas H. Goldhesh, Rag. No. 33,123; Moules Chie Mins, Reg. No. 36,105; Richard J. Berman, Reg. No. 39,107; King L. Wong, Rag. No. 37,500; Karen K. Costoriche, Reg. No. 33,107; James A. Pestos, III., Rag. No. 31,714; Parrich D. Muir, Règ. No. 37,405; Sharen N. Klesser, Reg. No. 36,335; and Marnt Chaps, Reg. No. 44,275; Bratley D. Goldines, Reg. No. 43,637; and N. Alexander Nelte, Reg. No. 45,689.

運液電流運輸先: (名前及び電影番号)

Please direct all communications to the following address: ARENT FOX KINTNER PLOTKIN & KAHN, PLLC 1050 Connecticut Avenue, N.W., Suite 600 Washington, D.C. 20036-5339 Tol: (202) 857-6000; Fax: (202) 857-6395

権一当たは第一会明書名		Full name of sole or first strenger Yoshihiro Takemae
会明者の著名	自付	inventors signature Outs Jan. 21, 20
生 所		Residence Kasugai, Japan
亚 两		Crizzensnip JAPAN
私事用		Prox Office Address c/o FUJITSU VLSI LIMITED 1844-2, Kozoji-cho 2-chome,
		Kasugai-shi, Aichi 487-0013 Japan
第二共同発明者名		Full name of second joint inventor, if any
第二共同発明者の署名	日村	Second inventor's signature Date
色所	 ,	Residence
亞灣	·····	Cittzenenip
私書箱		Post Office Address
		

(第三以降の井周発明者についても同様に正故し、暮るをすること)

[Supply similar information and signature for third and subsequent joint inventors.)

EXHIBIT

Matsui et al.				
[54]		and apparatus for NG A Pattern		
[75]	Inventors:	Shongo Matsul, Sagamihara; Yoshimitu Mashima, Kawasaki; Kenichi Kobayashi, Tokyo, all of Japan		
[73]	Assignee:	Fujitsu Limited, Kawasaki, Japan		
[21]	Appl. No.:	409,983		

Aug. 20, 1982

Foreign Application Priority Data

Aug. 20, 1981 [JP] Japan 56-131276

Int. Cl.³ G01N 21/86

250/556, 560; 358/101, 106; 356/490, 376

[22] Filed:

[30]

United States Patent [19]

[11]	Patent Number:	4,
[45]	Date of Patent:	Jul

4,527,070 Jul. 2, 1985

[56]	References Cited

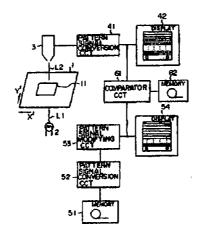
U.S. PATENT DOCUMENTS			
4,390,955	5/1983	Yoshida	358/101
4,414,566 1	1/19 8 3		358/101

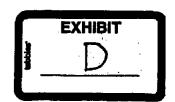
Primary Examiner—David C. Nelms Assistant Examiner—J. Jon Brophy Attorney, Agent, or Firm—Stazz & Halsey

[57] ABSTRACT

In a method for inspecting a pattern produced by using pattern data of a predetermined reference pattern, comparison is carried out between the pattern reproduced from the scanning signal of the pattern and the pattern produced from the signal of a modified form of the predetermined reference pattern.

12 Claims, 8 Drawing Figures





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Dkt. No. 22.1550/CMK

NTAL DECLARATION AFTER ALLOWANCE

we, SHOUGO MATSUI, YOSHIMITU MASHIMA and KENICHI KOBAYASHI, residing at 1609-33, Sobudaidanchi, Sagamihara-shi, Kanagawa 229, Japan; Suehiroso, 1743, Shimonumabe, Nakahara-ku, Kawasaki-shi, Kanagawa 211, Japan and 6-34-3, Nagasaki, Toshima-ku, Tokyo 171, Japan, declare that we are citizens of JAPAN and we are the same individuals who on or about August 11, 1982 executed a combined Declaration and Power of Attorney accompanying the subject U.S. Patent Application entitled METHOD AND APPARATUS FOR INSPECTING A PATTERN, which was filed August 20, 1982 and assigned U.S. Serial No. 409,983. We have reviewed and understand the amendments to the subject application, and we declare that we are the original and first inventors of the invention as now described and claimed therein.

We declare that all statements made herein of our own knowledge are true, that all statements made on information and belief are believed to be true, that these statements and the like so made are punishable by fine or imprisonment or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the subject application or any patent issuing thereon.

Dated April 4, 1985 Shouge Matsui

Dated April 4, 1985

Yoshimitu Mashima
YOSHIMITU MASHIMA

.

Dated April 4, 1985 | Kenichi Kobayashi | KENICHI KOBAYASHI



[56]

United States Patent [19]

Takagi et al.

[30]

[11] Patent Number:

4,539,068

[45] Date of Patent:

Sep. 3, 1985

[54]	VAPOR P	hase growth method	
[75]	Inventors:	Mikio Takegi, Kawasaki, Kanetake Takasaki, Tokyo; Kenji Koyama, Yokosuka, ali of Japan	
[73]	Assignee:	Pujitsu Limited, Kawasaki, Japan	
[21]	Appl. No.:	412,260	
[22]	Filed:	Aug. 27, 1982	
	Relat	ted U.S. Application Data	
[63]	Continuation of Ser. No. 264,805, May 18, 1981, abandoned, which is a continuation-in-part of Ser. No. 184,363, Sep. 5, 1980, abandoned.		

Foreign Application Priority Data

[52] U.S. Cl. 156/614; 427/93;

[58] Field of Search 156/614, 613, DIG. 64,

156/DIG. 99; 423/349; 148/175; 427/34, 39,

86, 94, 93, 95, 248.1, 255.2, 87; 204/192 S, 177,

427/94; 156/DIG. 64

Sep. 20, 1979 [JP] Japan 54-121489

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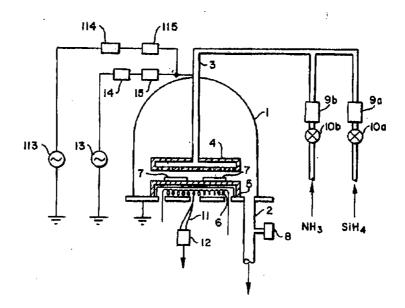
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Primary Examiner—Hiram H. Bernstein Attorney, Agent, or Firm—Stans & Halsey

[57] ABSTRACT

A plasma chemical vapor deposition method for forming a film on a substrate which is placed on one of a pair of electrodes oppositely arranged within the reaction chamber of a reactor. A plurality of power generators of different frequencies are applied to the electrodes to excite reactive gases introduced into the reaction chamber, whereby the reactive gases are transformed into a plasma and a desired film is formed on the substrate. Film with a small number of pinholes was formed at a relatively high deposition rate by combinations of power generator frequencies of, for example, 13.56 MHz and 1 MHz, 13.56 MHz and 50 KHz, and 5 MHz and 400 KHz.

3 Claims, 10 Drawing Figures







Dkt. No. 21.1071-CIP/C/JCG

SUPPLEMENTAL DECLARATION AFTER ALLOWANCE

We, MIKIO TAKAGI, KANETAKE TAKASAKI and KENJI KOYAMA, residing at 6-20-3, Nagao, Tama-ku, Kawasaki-shi, Kanagawa 213, Japan; 2-26-10-703, Ohmorikita, Ohta-ku, Tokyo 143, Japan; and 3-56, Higashihemi-cho, Yokosuka-shi, Kanagawa 238, Japan, declare that we are citizens of JAPAN and we are the same individuals who on or about May 13, 1981 executed a combined Declaration and Power of Attorney accompanying the subject U.S. Patent Application S.N. 264,805 entitled VAPOR PHASE GROWTH METHOD AND APPARATUS, which was filed on May 18, 1981 which is a continuation-in-part of U.S. Serial No. 184,363 filed September 5, 1980, the subject application being a continuation of U.S. Serial No. 264,805, assigned U.S. Serial No. 412,260 and filed August 27, 1982. We have reviewed and understand the amendments to the above applications, and we declare that we are the original and first inventors of the invention as now described and claimed therein.

We declare that all statements made herein of our own knowledge are true, that all statements made on information and belief are believed to be true, that these statements and the like so made are punishable by fine or imprisonment or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the subject application or any patent issuing thereon.

Mikio Takagi Dated June 5, 1985

Dated June 5, 1985

Dated June 5, 1985

EXHIBIT

	nited S	tates Patent [19]
[54]		DUCTOR MEMORY DEVICE STACKED CAPACITOR-TYPE CELLS
[75]	Inventors:	Yoshihire Takemae, Tokyo; Tomio Nakano, Kawasaki; Kimiaki Sato, Tokyo, all of Japan
[73]	Assignee:	Pujitsu Limited, Kawasaki, Japan
[21]	Appl No.:	560,171
[22]	Filed:	Dec. 12, 1983
[30]	Foreign	Application Priority Data
Dec	. 20, 1982 [JF] Japan 57-222079
[51] [52]	Int. CL4 U.S. Cl	
(58)	Field of Sea	reh 357/23.6, 23.11, 51 357/24, 54
[56]		References Cited
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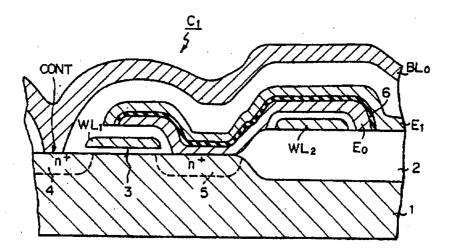
[11]	Patent Number:	4,641,166
[45]	Date of Patent:	Feb. 3, 1987

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		Japan
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Primary Exam	niner—b	fartin H. Bdlow
		Sara W. Crane
		m-Staas & Halsey
	ad AL Tal	UL JOHNSON OF THEMOSA

[57] ABSTRACT

In a semiconductor memory device having stacked capacitor-type memory cells, the capacitor of each memory cell comprises an electrode, an insulating layer, and a counter electrode. The electrode is connected electrically to a source or drain region of a transfer transistor and extends over a part of a word line adjacent to another word line serving a gate electrode of the transfer transistor, at which part no memory cell is formed.

10 Claims, 8 Drawing Figures





J.M.

Docket No. 22.1786/WDJ

SUPPLEMENTAL DECLARATION AFTER ALLOWANCE

We, Yoshihiro Takemae, Tomio Nakano, Kimiaki Sato, residing at 8-13-24-303, Akasaka, Minato-ku, Tokyo 107, Japan; 127-103 Sugsaengoku, Tama-ku, Kawasaki-shi, Kanagawa 214, Japan Rowsonski kwakik, Kanagawa ZKK, Japan and 4-11-35-204, Minamiazabu, Minato-ku, Tokyo 106, Japan respectively, declare that we are citizens of Japan and that we are the same individuals who, on or about 25 November 1983 executed a combined Declaration and Power of Attorney accompanying a U.S. patent application entitled SEMICONDUCTOR MEMORY DEVICE HAVING STACKED CAPACITOR-TYPE MEMORY CELLS, which was filed 12 December 1983 and assigned Serial No. 560,171. We have read all amendments to the specification and claims of the application, we understand the content of the invention as now described and claimed in the subject application and we declare that we are the original and first inventors thereof and further that this invention was completed before the filing of the subject application.

We acknowledge our duty to disclose information of which we are aware which is material to the examination of the subject application.

We declare further that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that false statements and the like so made are punishable by fine or imprisonment or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

September 1, 1986

September 1, 1986

September 1, 1986

September 1, 1986

Kimiaki Sato

Date

United States Patent 1191 Takemae [54] FET VOLTAGE REFERENCE CIRCUIT WITH THRESHOLD VOLTAGE COMPENSATION Yoshihiro Takemse, Tokyo, Japan [75] Inventor: [73] Assignee: Fujitsu Limited, Kawasaki, Japan [21] Appl. No.: 15,529 Feb. 12, 1987 [22] Filed: Related U.S. Application Data Continuation of Ser. No. 663,712, Oct. 22, 1984, aban-[63] Pereign Application Priority Data [30] Nov. 11, 1983 [JP] Japan 58-212083 307/304; 323/314; 323/349; 323/350; 365/226 [58] Field of Search 323/311, 313, 349, 350, 323/314; 307/296 R, 297, 304; 365/226 References Cited [56] U.S. PATENT DOCUMENTS 3,823,332 7/1974 Peryazka et al. 307/297

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Bell 330/293

[11] Patent Number:

4,692,689

[45] Date of Patent:

Sep. 8, 1987

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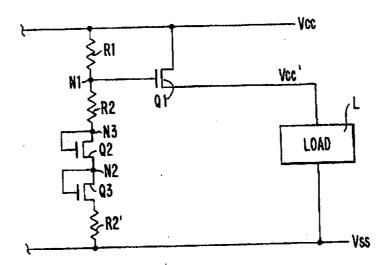
Askin et al., "FET Device Parameters Compensation Circuit", IBM Tech. Discl. Bul., vol. 14, No. 7, pp. 2088, 2089, Dec. 1971.

Primary Examiner-William H. Beha, Jr. Attorney, Agent, or Firm-Steas & Halsey

[57] ABSTRACT

A voltage converting circuit has an output MIS transistor which gives a low output impedance and outputs an intermediate level of power source voltage. The output level is set with a high accuracy through a voltage dividing ratio determined by an impedance element. This impedance element is connected with a compensating MIS transistor to compensate for variations of the gate threshold voltage caused by the manufacturing process.

10 Claims, 9 Drawing Figures





	nited State	es Patent	[19]
(54)		DOM ACCESS M CH CAPACITOR V LINED LOWER	
[75]	Inventor: Masa	o Tagucki, Sagamil	asra, Japan
[73]	Assignee: Fujita	u Limited, Kanaga	wa, Japan
[21]	Appl. No.: 16,61	1 .	
[22]	Filed: Feb. 1	19, 198 7	
[30]	Foreign Appl	ication Priority Da	ta
	b. 20, 1986 [JP] — Ja ar. 3, 1986 [JP] — Ja		
	Int. Cl. ⁴ U.S. Cl		23.6; 357/54;
[58]	Field of Search	357/23.0	6, 55, 59, 54; 365/149
[56]	Refe	rences Cited	
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4	4,672,410 6/1987 N	flara ot al	357/23.6
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[11]	Patent Number:	4,801,989
[45]	Date of Patents	Jan. 31, 1989

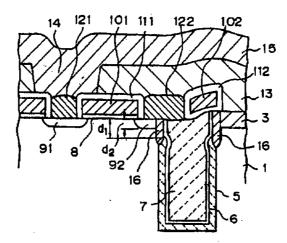
59-141262 60-14472	4/1984 of 1985	Japan .	357/23.6
60-34472 61-15362			

Primary Examiner—Joseph B. Clawson, Jr. Attorney, Agent, or Firm—Armstrong, Nikaido, Marmelstein & Kubovoik

[57] ABSTRACT

In a dynamic random access memory having a trench capacitor, a first conductive layer is formed on all of the inner surface of the trench except for a region adjacent to the opening portion of the trench, a dielectric layer is formed on the first conductive layer exposed in the trench and the surface of the semiconductor substrate, and a second conductive layer of the other conduction type is filled in the trench through the dielectric layer. The first conductive layer, the dielectric layer, and the second conductive layer constitute a storage capacitor. In this dynamic random access memory, a metal insulator semiconductor transistor is formed in the semiconductor substrate, a source or drain region of the transistor of the other conduction type is in contact with the second conductive layer through the dielectric layer, and the second conductive layer is connected with the source or drain region of the other conduction type.

8 Claims, 9 Drawing Sheets





Armstrong, Nik - Marmelstein & Kubovcik

Dec...cation For Patent Application

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	(check one) 😧 is attache	ed hereto.			
	was filed	on		_	
	Application Se	erial No.			
	and was amen	ded on	BF:	ipplicable)	•
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Prior	Foreign Application(s)	•			70 to 10 min 1 min
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[11] Patent Number: 5,227,996

Date of Patent:

Jul. 13, 1993

[54] SEMICONDUCTOR MEMORY DEVICE HAVING WORD LINE DRIVER

United States Patent [19]

[75] Inventor: Toshiya Uchida, Kawasaki, Japan

[73] Assignee: Fujitsu Limited, Kanagawa, Japan

[21] Appl. No.: 757,154

Uchida

[22] Filed: Sep. 10, 1991

[30] Foreign Application Priority Data

Sep. 14, 1990 [JP] Japan 2-244585 ... G11C 5/06

365/230.06

365/189.11

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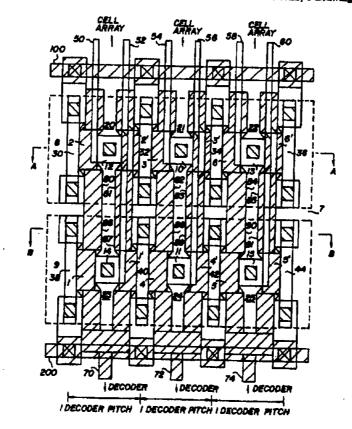
Primary Examiner-Eugene R. LaRoche

Assistant Examiner-Do Hyum Yoo Attorney, Agent, or Firm-Nikaido, Marmelstein, Murray & Oram

ABSTRACT

A semiconductor memory device includes first and second word lines which extend in parallel to each other, at least one line activation signal line which extends perpendicularly to the first and second word lines, a device isolation region which extends perpendicularly to the first and second word lines, a first driver for activating the first word line and having a first impurity region provided adjacent to the device isolation region and connected to the word line activation signal line, a first gate electrode and a second impurity region connected to the first word line, a second driver for activating the second word line and comprising a third impurity region provided adjacent to the device isolation region on an opposite side from the first impurity region and connected to the word line activation signal line, a second gate electrode and a fourth impurity region connected to the second word line, and a decoder connected to the first and second gate electrodes.

14 Claims, \$ Drawing Sheets





Declaration or U.S. Patent Applica in

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my same,

I believe I am the original, first and sole inventor (if only one name is jisted below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

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US005339273A

United States Patent [19]

Taguchi

[11] Patent Number:

5,339,273

[45] Date of Patent:

Aug. 16, 1994

[54]	HAVING A	TESTR	MEMORY D G FUNCTION FING THE SA	dia P
[75]	Inventor:	Masse T	aguchi, Kawas	aki, Japan
[73]	Assignee:	Fujiton l	idi, Kanagawa	, Japan
[21]	Appl. No.:	806,406		
[22]	Filed:	Dec. 13,	1991	
[30]	Foreig	n Applica	tion Priority D	ste
De	o. 1 4, 1990 [J.	P] Japan	t	2-410668
			G11C 29/0 365/	
[58]	Field of Se	urch	365/149, 365/	
[56]		Referen	nces Cited	
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Primary Examiner—Bugene R. LaRoche
Assistant Examiner—Son Dinh

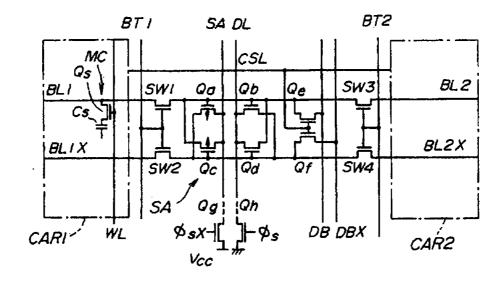
Attorney, Agent, or Firm—Armstrong, Westerman, Hattori, McLeland & Naughton

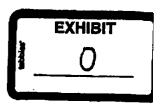
[57] ABSTRACT

A semiconductor memory device is provided with a plurality of bit lines, a plurality of word lines, a memory cell array including a plurality of memory cells each coupled to one bit line and one word line, and a varying part for varying a capacitance of at least a selected one of the bit lines in response to a predetermined signal

which indicates a test mode in which an operation of the semiconductor memory device is tested.

15 Claims, 7 Drawing Sheets

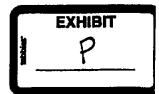




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Post Office Address Same as residence



United States Patent [19]

Konno et al.

Patent Number: [11]

5.397,432

[45] Date of Patent:

Mar. 14, 1995

[54]	METHOD FOR PRODUCING
	SEMICONDUCTOR INTEGRATED
	CIRCUITS AND APPARATUS USED IN
	SUCH METHOD

[75] Inventors: Jun-ichi Kenno, Kuwana; Keisuke Shinagawa, Kawasaki; Toshiyuki Ishida, Kawaraki; Takahiro Ito, Kawasaki; Tetsuo Kondo, Kawasaki; Fukashi Harada, Kuwana; Shuzo Fajimura, Tokyo, all of Japan

[73] Assignce: Fujitsu Limited, Kawasaki, Japan

[21] Appl. No.:

743,383

[22] PCT Filed:

Jun. 26, 1991

[86] PCT No.:

PCT/JP91/00861

§ 371 Date:

Aug. 21, 1991

§ 102(e) Date:

Aug. 21, 1991

[87] PCT Pub. No.:

WO92/00601

PCT Pub. Date: Jan. 9, 1992

[30] Foreign Application Priority Data

Jun. 21, 1990	[as] asban	
[51] Int. Cl. ⁶ . [52] U.S. Cl	1 04 0 50 0 11 11 10 10 10 10 10 10 10 10 10 10	H01L 21/06

156/646; 134/1 [58] Field of Search 156/643, 646, 664, 665, 156/666; 134/1

[56]

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61-147530 7/1986 Japan 1-30225 2/1989 Japan . 1-48421 2/1989 Japan . 1-239933 9/1989 Јареп 2-49425 2/1990 Japan 2-71519 3/1990 Japan 2/1990 Japan 2-144525 6/1990 Japan 2-165656 6/1990 Japan .

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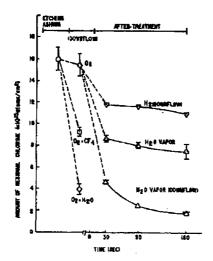
Primary Examiner -- R. Bruce Breneman Assistant Examiner-George Goudreau Attorney, Agent, or Firm-Nikaido, Marmeistein, Murray & Oram

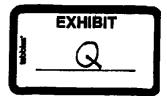
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ABSTRACT

To prevent after-corrosion of wiring or electrodes formed by patterning films of aluminum or an alloy thereof by reactive ion etching (RIE) using an etchant containing chiorine gas or its gaseous compounds, residual chlorine on the surface of the wiring or electrodes is removed by exposing it to a plasma generated in an atmosphere containing water vapor or to neutral active species extracted from the plasma. This treatment is performed either at the same time or after an ashing operation, an operation for removing a resist mask used in the aforesaid RIB by adding water vapor to an atmosphere containing oxygen. To perform the latter separate treatment, an automatic processing system is disclosed in which an after-treatment apparatus for removing residual chlorine is connected, via a second load lock chamber, to an ashing apparatus connected to a RIE apparatus by a load lock chamber which is capable of making a vacuum.

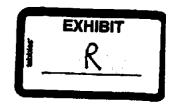
19 Claims, 6 Drawing Sheets





Declaration For U.S. Patent Application

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ISO05688712A

United States Patent [19]

Ema et al.

[11] Patent Number:

5,688,712

(45) Date of Patent:

Nov. 18, 1997

[54]	PROCESS FOR PRODUCING A SEMICONDUCTOR DEVICE

- [75] Inventors: Taiji Emn; Toshimi Ikeda, both of Kawasaki, Japan
- [73] Assignee: Fujitsu Limited, Kanagawa, Japan
- [21] Appl. No.: 643,938
- [22] Filed: May 7, 1996

Related U.S. Application Data

[62] Division of Set. No. 376,082, Jan. 20, 1995, Pat. No. 5,550,395, which is a continuation of Set. No. 46,149, Apr. 15, 1993, abundoned.

[52] U.S. Cl. 437/60; 437/52; 437/49; 437/195; 437/228; 437/236

[58] Field of Search 437/60, 47, 48, 437/49, 51, 52, 189, 195, 228, 235, 236

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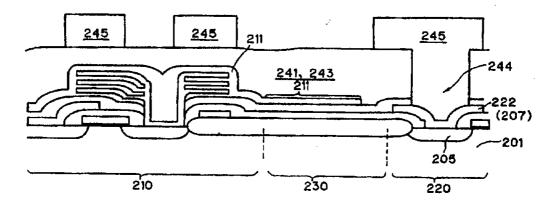
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Primary Examiner—Tuan H. Nguyen
Attorney, Agant, or Firm—Nikaido Marmelstein Murray &
Oram LLP

[57] ABSTRACT

A semiconductor device includes a semiconductor substrate having a memory cell area and a circuit area surrounding the memory cell area with a boundary area interposed therebetween. A first conductive layer covers the memory cell area and extends onto the boundary area. A first insulating layer covers the aurrounding circuit area and part of the extended portion of the first conductive layer. A second insulating layer covering the first insulating layer and the first conductive layer. A throughhole is formed through the first and second insulating layers. A second conductive layer is electrically connected with another conductive layer via the throughhole and extends from the memory cell area to the surrounding circuit area. The process of producing the semiconductor device is also disclosed.

\$ Claims, 1\$ Drawing Sheets





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5,841,731

Shinozaki

1451 Date of Patent:

Nov. 24, 1998

[54]	SEMICONDUCTOR DEVICE HAVING EXTERNALLY SETTABLE OPERATION
	MODE

United States Patent [19]

[75] Inventor: Naoharu Shinozaki, Kawasaki, Japan

[73] Assignce: Fujitsu Limited, Kawasaki, Japan

[21] Appl. No.: 862,298

[22] Filed: May 22, 1997

[30] Foreign Application Priority Data

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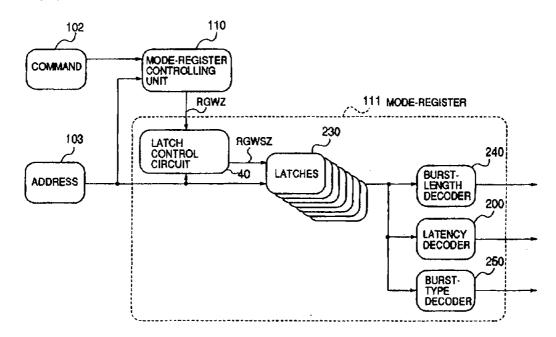
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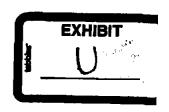
Primary Examiner—David C. Nelma
Assistant Examiner—Hien Nguyon
Attorney, Agent, or Pirm—Nikaido, Marmelstein, Murray &
Oram LLP

[57] ABSTRACT

A semiconductor device which allows an input signal thereto to select one of N operation modes, and operates in the one of N operation modes includes a selection circuit for selecting an operation mode from the N operation modes when the input signal indicates the operation mode, and for selecting a predetermined operation mode from the N operation modes when the input signal is an undefined signal indicating none of the N operation modes. The semiconductor device further includes an internal circuit operating in an operation mode selected by the selection circuit.

11 Claims, 8 Drawing Sheets .





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Dec. . ation For U.S. Patent expelication

As a below named inventor, I hereby declars that:

My residence, post office address and citizenship are as stated below my name.

Joseph over 1 are the original, first and sole inventor (if only one name is fisted below) or an original, first and joint inventor (if phr names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention subject matter which is claimed and for which a patent is sought on the invention subject (Insert Title) SEMICENDICTOR DEVICE AVOIDING MALFUNCTION CAUSED BY ILLEGAL INPUT

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US006104486A

United States Patent [19]

Arimoto

6,104,486 [11] Patent Number: *Aug. 15, 2000 Date of Patent:

[54] FABRICATION PROCESS OF A SEMICONDUCTOR DEVICE USING **ELLIPSOMETRY**

[75] Inventor: Hiroshi Arimoto, Kawasaki, Japan

[73] Assignee: Fujitsu Limited, Kawasaki, Japan

[*] Notice: This patent issued on a continued prosecution application filed under 37 CPR 1.53(d), and is subject to the twenty year

patent term provisions of 35 U.S.C.

154(a)(2).

[21] Appl. No.: 08/774,272

Dec. 27, 1996 [22] Filed:

[30] Foreign Application Priority Data

[52] U.S. Cl. 356/300; 356/305; 356/310; 356/322; 356/337; 356/340; 356/345; 356/351; 356/364; 356/128; 250/492.1; 250/492.2; 250/492.22; 250/492.3

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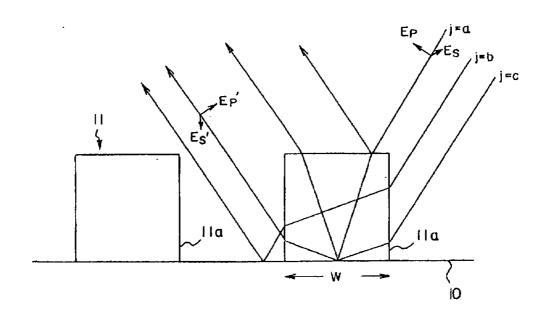
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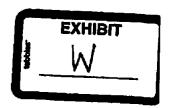
Primary Examiner-Christopher L. Chin Assistant Examiner-Bao-Thuy L. Nguyon Attorney, Agent, or Firm-Armstrong, Westerman, Hattori, McLeland & Naughton

ABSTRACT [57]

A method of fabricating a semiconductor device includes the steps of illuminating a structure formed on a surface of a substrate by an incident optical beam incident to the structure with a predetermined incident angle with respect to the surface, measuring a polarization state of an exiting optical beam exiting from the structure in response to an illumination of the structure by the incident optical beam, and evaluating a size of the structure in a direction parallel to the surface from the polarization state of the exiting optical beam, and adjusting a parameter of production of a semiconductor device in response to the size.

11 Claims, 24 Drawing Sheets





(12) United States Patent

Tomita et al.

(10) Patent No.:

US 6,292,428 B1

(45) Date of Patent:

Sep. 18, 2001

EXHIBIT

SEMICONDUCTOR DEVICE RECONCILING DIFFERENT TIMING SIGNALS

- (75) Inventors: Hiroyoshi Tomita; Tatsuya Kanda, both of Kawasaki (JP)
- (73) Assignee: Fujitsu Limited, Kanagawa (JP)
- (*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.
- (21) Appl. No.: 09/240,007
- (22) Filed: Jan. 29, 1999

(30)Foreign Application Priority Data

(JP) 10-022257	Feb. 3, 1998	
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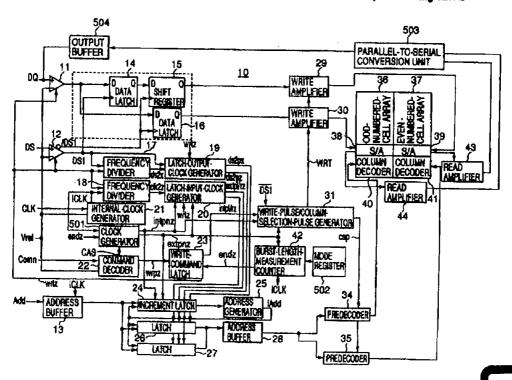
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Primary Examiner-Huan Hoang (74) Attorney, Agent, or Pirm-Arent Fox Kintner Plotkin & Kahn, PLLC

ABSTRACT

A semiconductor device which receives addresses in synchronism with a clock signal and receives data in synchronism with a strobe signal includes address-latch circuits, a first control circuit which selects one of the address-latch circuits in sequence in response to the clock signal, and controls the selected one of the address-latch circuits to latch a corresponding one of the addresses in response to the clock signal, and a second control circuit which selects one of the address-latch circuits in sequence in response to the strobe signal, and controls the selected one of the address-latch circuits to output a corresponding one of the addresses in response to the strobe signal.

42 Claims, 25 Drawing Sheets



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(12) United States Patent Tomita et al.

(10) Patent No.:

US 6,320,819 B2

(45) Date of Patent:

Nov. 20, 2001

(54) SEMICONDUCTOR DEVICE RECONCILING DIFFERENT TIMING SIGNALS

(75) Inventors: Hiroyoski Tomita; Tatsuya Kanda, both of Kawasaki (JP)

(73) Assignce: Fujitsu Limited, Kawasaki (JP)

Subject to any disclaimer, the term of this (*) Notice: patent is extended or adjusted under 35

U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/733,961

Dec. 12, 2000 (22) Filed:

Related U.S. Application Data

Division of application No. 09/240,007, filed on Jan. 29, (62)1999.

(30) Foreign Application Priority Data	(30)
Feb. 3, 1998 (JP) 10-022257	Feb
(51) Int. CL ⁷	(51) (52)
(58) Field of Search	(58)

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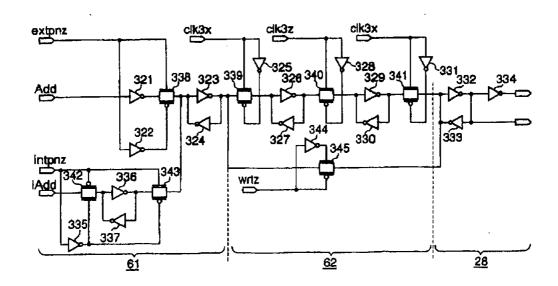
* cited by examiner

Primary Examiner-Huan Houng (74) Attorney, Agent, or Firm-Arent Fox Kintner Plotkin & Kahn PLLC

ABSTRACT (57)

A semiconductor device which receives addresses in synchronism with a clock signal and receives data in synchronism with a strobe signal includes address-latch circuits, a first control circuit which selects one of the address-latch circuits in sequence in response to the clock signal, and controls the selected one of the address-latch circuits to latch a corresponding one of the addresses in response to the clock signal, and a second control circuit which selects one of the address-latch circuits in sequence in response to the strobe signal, and controls the selected one of the address-latch circuits to output a corresponding one of the addresses in response to the strobe signal.

6 Claims, 25 Drawing Sheets



365/230.08, 194

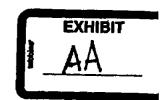
EXHIBIT

N, M, M & O' Docket No. . NIKAIDO, MARMILITIMA SERAY & ORAM LLP Declaration For U.S. Patent Application As a below sussed inventor, I hereby declare that: My residence, post office address and citizenship are as mated below my name. I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sometic on the investion estimated (insert Title) SEMICONDUCTOR DEVICE RECONCILING DIFFERENT TIMING SIGNALS the specification of which (Check or of Monks 1, 2 or 3. · I. 💢 is attached hereto. 2. 🗆 was filed on International PCT Application Social No. See mate A on back of this page) and was amended on (if applicable) 13. C was filed on U.S. Application Serial No. and was assended on (Mapplicable) I hereby state that I have reviewed and understand the contents of the shove-identified specification, including the claim(s), en amended by any amendment referred to above. I acknowledge the daty to disclose information which is material to the examination of this application is accordance with Title 37, Code of Pederal Regulations, \$1.56(a). I increby claims foreign priority benefits under This 35, United States Code, §119 of any foreign application for patent or inventor's circlicate listed below and lawye stee identified below any foreign application for patent or inventor's certificate having a filing date before that of stojapplication for which priority is cisimed: Priority Claimed 1,1 Pat. Appln. No.10-022257 Japan 3/February/1998 XYes CI No ш (Number) (Country) (List peter (Day/Month/Year Piled) 41 ☐ Yes ☐ No 111 (Number) (Country) (Day/Month/Year Flied) ☐ Yes ☐ No Number (Country) (Day/Month/Year Flied) þib See attached list for additional prior fereign applications Ш I hereby claim the benefit under Tide 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the masser M provided by the first paragraph of Title 35, United States Code, \$112, I seknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, \$1.56(a) which occurred between the filling date of the prior application and the national or PCT international filling date of this applications (List priet U.S. Applications) (Application Serial No.) (Piling Date) (Status) (patented, pending, abandoned) (Application Serial No.) (Piting Date) (Stram) (patented, pending, abandoned) And I hereby appoint as principal attornays David T. Nikaide, Reg. No. 22,663; Charles M. Marmelstein, Reg. No. 25,893; George H. Oram, Jr., Rag. No. 27,931; Rabert B. Marray, Rag. No. 22,980; Martin S. Postman, Roy. No. 18,570; E. Marcin Emas, Reg. No. 32,131; Douglas H. Goldhush, Rag. No. 33,125; Kevin C. Brown, Reg. No. 32,402; Monica Chin Kitta, Reg. No. 36, 105; Sharon N. Klesner, Reg. No. 36,335 and Richard J. Berman, Reg. No. 39,107. Please direct all communications to the following address: NEKAIDO, MARMELSTEIN, MURRAY & ORAM LLP Metropolitan Square 655 Pifteenth Street, N.W., Suite 330 - G Street Lobby Washington, D.C. 20065-5701 (202) 638-5000 Pax: (202) 638-4810 I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and ballef are believed to be true; and further that these statements were made with the knowledge that willful false state

like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any pasent issued thereon.

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cyn baffe)	Inventor's signature things who to mite	Jan. 25, 1999
	Residence Kawamaki-shi, Kanagawa, Japan	Date
	Chizonthip Japan	

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10 11	Attorneys for Plaintiffs Nanya Technology Corp. and Nanya Technology Corp. U.S.A.					
12 13	UNITED STATES DISTRICT COURT					
14	DISTRICT OF GUAM					
15						
16	NANYA TECHNOLOGY CORI NANYA TECHNOLOGY CORI		Case No. CV-06-0002	2.5		
17	Plaintiffs,		CERTIFICATE OF	SERVICE		
18	v.					
19	FUJITSU LIMITED and FUJITS	SII.				
20	MICROELECTRONICS AMER					
21	Defendan	ts.				
22	I, JOSEPH C. RAZZANO, Esq., hereby declare as follows:					
23	1. I am over the age of majority and am competent to testify regarding the matters stated					
24	herein.					
25	2. I hereby certify	that on May 3, 200	07, a true and exact	copy of PLAINTIFFS'		
26		•	·	••		
27	RESPONSE TO DEFENDANT	13 MOHON IO IIV	IMEDIAIELI IKAN	SEER FOR CONVEN-		
28		- 1-				
	PLAINTIFFS' RESPONSE TO DEF TO IMMEDIATELY TRANSFER F					

IENCE was served via hand delivery on Defendant Fujitsu, Ltd. through its attorneys of record, Calvo & Clark, at their offices located at 655 South Marine Corp. Drive, Tamuning, Guam 96913.

3. I declare under penalty of perjury that the foregoing is true and correct.

DATED at Sinajana, Guam on May 3, 2007.

JOSEPH C. RAZZANO, JSQ.